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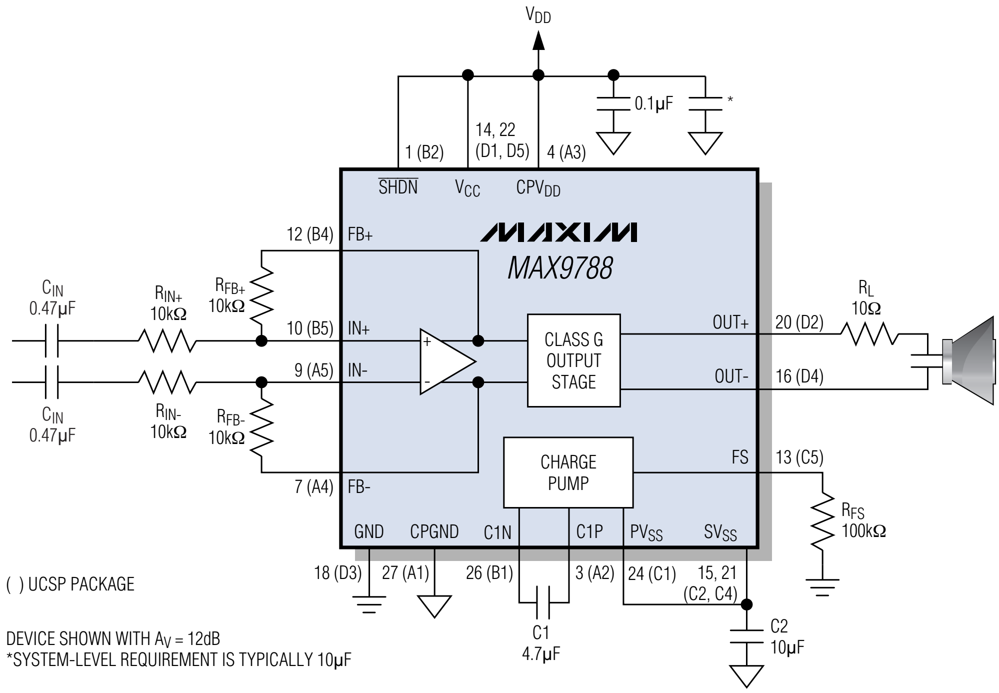

The MAX9788 is shown in a typical ceramic speaker application circuit. (See page 5.)

Letter from the CEO

Innovation and Availability

For 25 years, Maxim has gained a well-deserved reputation for innovation. During that time, we introduced more new products than any other analog and mixed-signal company, and our rate of introduction currently averages just over one new product every business day. Innovative thinking is embedded in our culture, and it permeates all levels of the company.

There were periods during the past decade that our customers would say, "Maxim makes great products, if only we could get them delivered on time!" We took major steps during the last couple of years to eliminate the problem and improve our reputation. The most fundamental step is not visible, but it is the most important: *we changed our attitude towards delivering your product*. We made it a major company initiative to improve timely delivery of products, and our employees have responded with enthusiasm. My objective is to ingrain on-time delivery within our culture alongside innovation.

We have also taken other, more visible steps to improve deliveries.

1) We increased our wafer fab factory space by 80% in 2007, and we invested approximately $280 million in manufacturing and testing capacity.

2) We reduced manufacturing cycle time by 30% in the last nine months.

3) We put in place strategic inventory to meet demand for small prototyping and preproduction orders (< 100 pieces). We are now delivering 97% of those orders to customers within one week of the request date.

4) We are investing $25 million to upgrade our Enterprise Resource Planning (ERP) system for more accurate planning.

We regularly evaluate every aspect of our development and manufacturing processes, constantly looking for innovative ways to reduce the time it takes to define, design, fabricate, and test our products.

We have made noticeable improvement already, and we still have some distance to go, but you should already be finding it much easier to get Maxim parts whenever you want them, no matter the quantity.

We are always at your service,

Tunç Doluca
President and Chief Executive Officer

Amplifier Considerations in Ceramic Speaker Applications

By Mark Cherry, Corporate Applications Engineer

Today's portable devices need smaller, thinner, more power-efficient electronic components. Cellular phones have become so thin that the dynamic speaker is now the limiting factor in how thin manufacturers can make their handsets. The ceramic, or piezoelectric, speaker is quickly emerging as a viable alternative to the dynamic speaker. These ceramic speakers can deliver competitive sound-pressure levels (SPLs) in a thin and compact package, thus potentially replacing traditional voice-coil dynamic speakers. Some of the differences between dynamic and ceramic speakers are shown in **Table 1**.

Amplifier circuits that drive ceramic speakers have different output-drive requirements than those that drive traditional dynamic speakers. The structure of the ceramic speaker requires the amplifier to drive a large capacitive load and supply increasingly larger currents at higher frequencies while maintaining a high output voltage.

Ceramic Speaker Attributes

Ceramic speaker manufacturers use technology similar to that of building multilayer ceramic capacitors. This manufacturing technique gives speaker manufacturers tighter control over the speaker tolerances as compared to dynamic speakers. Tight construction tolerances become important when attempting to equalize the speaker, and are significant for obtaining repeatable sonic characteristics from unit to unit.

Ceramic speaker impedance, as seen by a driving amplifier, can be modeled as an RLC circuit with a large capacitance as its main element (**Figure 1**). Across most audio frequencies, the ceramic speaker is mostly capacitive. The speaker's capacitive nature dictates that impedance decreases as the frequency increases. **Figure 2** shows the similarity of ceramic speaker's impedance versus frequency to that of a 1μF capacitor. This impedance also has a point of resonance above which the speaker is most efficient at producing sound. The dip in impedance around 1kHz indicates the speaker's resonant frequency.

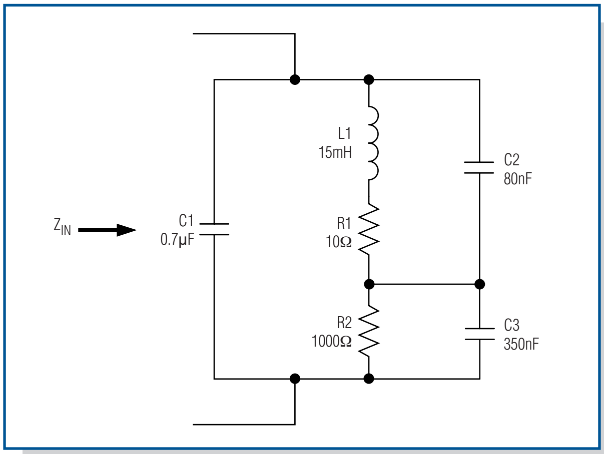

Figure 1. Ceramic speaker impedance has a large capacitance as its main element.

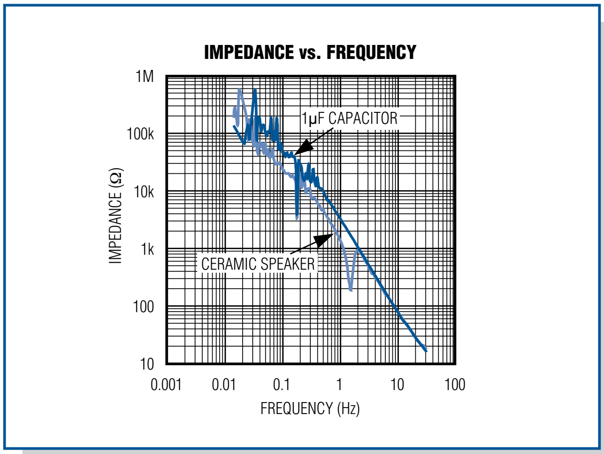

Figure 2. The impedance versus frequency of a ceramic speaker is very similar to that of a 1μF capacitor.

Table 1. Advantages and Disadvantages of Ceramic and Dynamic Speakers

Ceramic Speakers		Dynamic Speakers	
Advantages	**Disadvantages**	**Advantages**	**Disadvantages**
• High efficiency • Very thin form factor • Tight manufacturing tolerances • Smaller acoustic cavity required	• Large drive voltage required • Restricted low-frequency response • Capacitive load	• Inexpensive • Proven technology • Smooth frequency response	• Wide manufacturing tolerances • Inefficient • Thick solution size • Larger acoustic cavity required

Sound Pressure versus Frequency and Amplitude

An alternating voltage placed across the terminals of a ceramic speaker causes the piezoelectric film inside the speaker to deform and vibrate; the amount of displacement is proportional to the input signal. The vibrating piezoelectric film moves the surrounding air, thus producing sound. Increasing the voltage across the speaker increases the piezoelectric element deflection, creating more sound pressure and, therefore, increased volume.

Ceramic speaker manufacturers typically rate their speakers with a maximum terminal voltage, typically around $15V_{P-P}$. This maximum voltage is the point at which a ceramic element reaches its excursion limits. Applying a voltage that is greater than the rated voltage does not result in more sound pressure, but it does increase the amount of distortion present in the acoustic output signal. **Figure 3** shows a graph of a ceramic speaker's output sound-pressure level (SPL) versus frequency when driven with a maximum voltage.

By comparing the graphs of SPL versus frequency and impedance versus frequency, it is apparent that the piezoelectric speaker is most efficient at producing high SPLs above its self-resonant frequency.

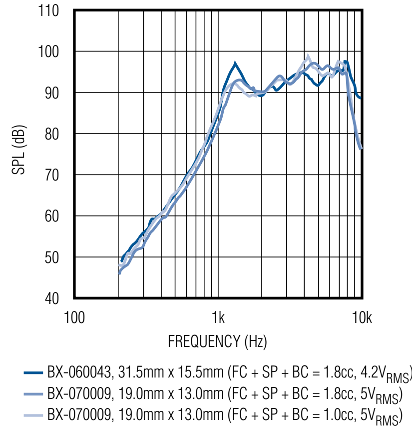

Figure 3. Output signal distortion increases when a voltage is applied that is greater than the speaker's rated voltage.

Amplifier Requirements when Driving a Ceramic Speaker

Ceramic speaker manufacturers specify a maximum voltage of $14V_{P-P}$ to $15V_{P-P}$ to produce the highest levels of sound pressure. The question quickly becomes how to generate these voltages from a single battery supply. One solution is to use a switching regulator to boost the battery voltage to 5V. Armed with a regulated 5V supply, the system designer could choose a single-supply amplifier that requires a bridge-tied load (BTL). Bridge-tying the load automatically doubles the voltage that the speaker perceives. However, supplying a BTL amplifier with a single 5V supply allows the output to only theoretically swing to $10V_{P-P}$. This voltage does not allow the ceramic speaker to output its highest SPL. To create higher SPLs, the power supply must be regulated to a higher voltage.

Another approach that employs a boost converter to regulate the battery voltage up to 5V or more has its own set of issues—namely the size of the components needed. Large peak inductor currents can quickly limit how small a total solution can be, because the inductor must be physically large so that the core does not saturate. High-current, small-profile inductors are available. However, the core's saturation current rating for these inductors may not be high enough to handle the load current needed to drive the speaker with high voltage at a high frequency.

High current drive and current-limit avoidance are needed to drive the ceramic element. This is because ceramic speakers have very low impedance at high frequencies. The amplifier used to drive a ceramic speaker must have enough current drive available so that it does not go into a current-limit mode when a large amount of high-frequency content is driven into the speaker.

Figure 4 shows an applications circuit using a MAX9788 Class G amplifier. Class G amplifiers have two voltage rails, one high and one low. The low-voltage rail is used when the output signal is small. The high-voltage rail is switched onto the output stage when the output signal demands a higher voltage swing. Because of its lower power-supply rail, the Class G amplifier is more efficient than a Class AB amplifier when the output signal is small. The Class G amplifier can still handle peak transients because of the higher available rail.

The MAX9788 shown in Figure 4 uses an on-chip charge pump to generate a negative rail that is the inverse of V_{DD}. This negative rail is only applied to the output stage when the output signal demands the higher rail. This device provides a more efficient method of driving a ceramic speaker than traditional methods that use a Class AB amplifier with a boost converter.

Speaker manufacturers always recommend a fixed resistance (R_L) in series with the ceramic speaker, as shown in Figure 4. This resistor acts to limit the amplifier's current output when the signal contains a great deal of

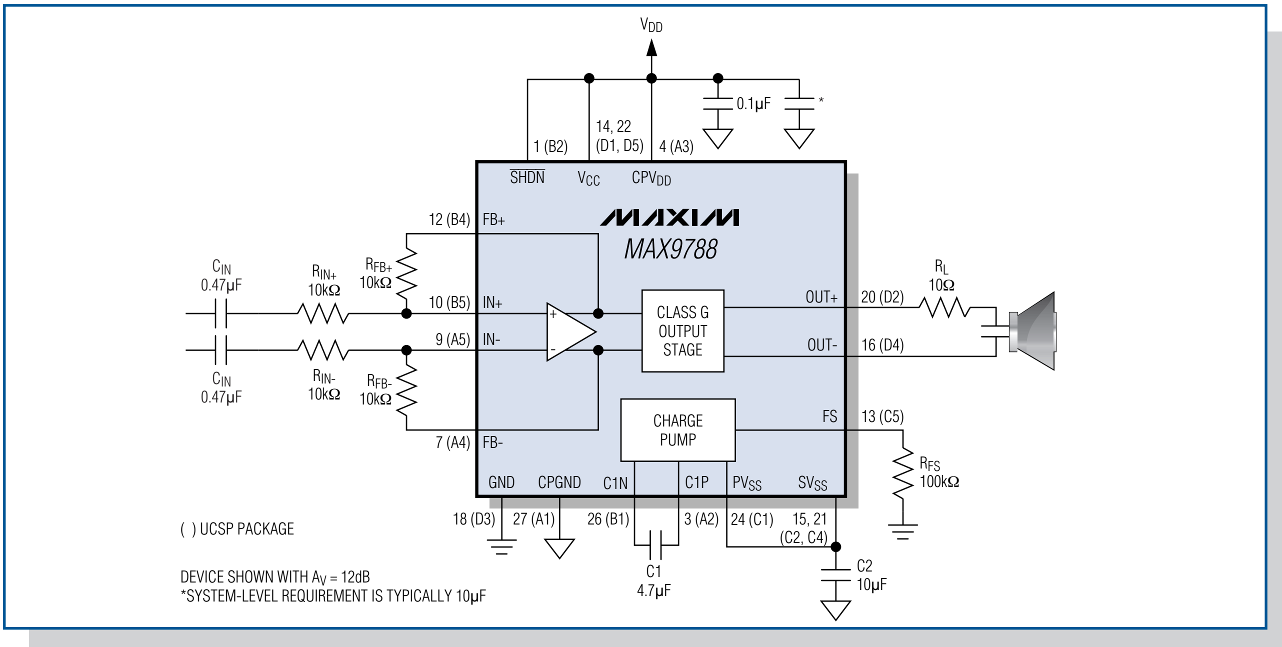

Figure 4. The MAX9788 is shown in a typical ceramic speaker application circuit.

high-frequency content. In some applications, fixed resistance may not be needed if the frequency response of the audio signal passed to the speaker can be bandwidth limited. This would ensure that the speaker does not look like a short circuit to the amplifier.

Contemporary ceramic speakers have a capacitance of approximately 1μF. The impedance of the Figure 4 speaker is 20Ω at 8kHz and 10Ω at 16kHz. Future ceramic speakers may have a larger capacitance that will force amplifiers to deliver even more current for the same signal frequency.

Efficiency in Ceramic Speakers vs. Dynamic Applications

Efficiency in a traditional dynamic speaker application is easy to calculate. The voice coil windings can be modeled electrically as a fixed resistance in series with a high-value inductance. Calculating power (P) delivered to the load is an Ohm's law problem using the resistance value of the speaker: $P = I^2R$, or P = V x I. Much of the power delivered to the speaker is dissipated as heat in the speaker coil.

Due to their capacitive nature, ceramic speakers do not generate very much heat when they dissipate power. Ceramic speakers dissipate a "blind" power. This is a very small amount of power based on the ceramic element's dissipation factor. Very little heat is generated when blind power is dissipated. Calculating blind power is not as straightforward as P = V x I;[1] instead, it is calculated as:

$$P = (\pi f C V^2) \times (\cos\varphi + DF)$$

Where:

C = capacitance value of the speaker

V = RMS drive voltage

f = frequency of the drive voltage

cosφ = phase angle between the current through the speaker and the voltage across the speaker

DF = dissipation factor of the speaker; this is quite low and depends on the signal's frequency and the ceramic speaker's ESR

Because the phase angle between the voltage and current is 90° in an ideal capacitor and the ceramic speaker is mostly capacitive, cosφ is equal to zero and causes no power dissipation in the capacitive portion of the ceramic speaker model. Imperfections in the ceramic material and dielectric cause the voltage across the speaker to lag behind the current through the speaker by a phase angle that does not quite equal 90°. This small difference between the ideal 90° phase shift and the actual phase shift is the dissipation factor (DF).

DF in a ceramic speaker can be modeled as a small, effective series resistance (ESR) in series with the ideal capacitor. Series resistance should not be confused with the isolation resistor that is placed in between the amplifier and the speaker. DF is the ratio of the ESR to the capacitive reactance at the frequency of interest:[2,3]

$$DF = R_{ESR} / X_C$$

For example, a ceramic speaker with a capacitance of 1.6μF and an ESR of 1Ω being driven by a $5V_{RMS}$, 5kHz signal would have a blind power of:

$$P = (\pi \times 5000 \times 1.6e^{-6} \times 5^2) \times (0 + 0.05) = 31.4mW$$

Real Power Dissipation

Though a ceramic speaker itself does not dissipate real power as heat like dynamic speakers do, heat is generated in the driving amplifier's output stage and in the external resistor (R_L) placed between the amp and the speaker (Figure 4). The larger the external resistor, the more power dissipation is moved off of the amplifier, at the expense of low-frequency response.

When driving a ceramic speaker with a 10Ω series resistor, one can see that blind power is a small contribution to the overall load power. Most of the power is dissipated in the external resistor, as shown by the required amplifier power delivery versus frequency graph in **Figure 5**.

Better low-frequency response requires a smaller external resistor, but that causes the amplifier's output stage to dissipate more power. Amplifier efficiency dictates how much power is dissipated in the amplifier's output stage. The need to dissipate power in the amplifier drives the need for more efficient solutions, including Class D and Class G amplifiers. The load consists of series resistance that leads to power dissipation in the load network, though not in the speaker. Even with a 100% efficient amplifier, a series resistor will burn power that is intended for the speaker.

In the Figure 5 example, at 5kHz, the total power delivered to the load is 629mW. An amplifier with 53% efficiency dissipates 558mW. The amount of power that the amplifier needs to dissipate dictates what size package the application can use. A significant amount of power dissipation is needed if high-frequency sine waves must be driven into the ceramic speaker.

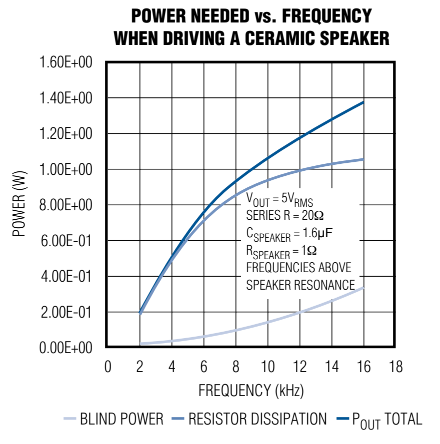

Figure 5. Blind power is a very small portion of the overall ceramic speaker load power; the majority of the power is dissipated in the external resistor.

Conclusion

Increasingly thinner portable devices are driving a need for low-profile ceramic speakers. These speakers are different than traditional dynamic speakers, so a different set of design considerations apply. The ceramic speaker's capacitive nature requires that the amplifier have a high output voltage and a large output current so that high voltage can be maintained over frequency. An amplifier chosen to drive a ceramic speaker must be able to deliver both blind and real power to the complex load. Amplifier efficiency must be high enough to allow for a small solution size and low cost. Such demands require the use of different amplifier topologies than the traditional Class AB amplifier. More efficient solutions like Class G or Class D amplifiers are becoming more attractive, with Class G amplifiers offering the best balance between solution cost, component count, and efficiency.

References

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Addressing the Physical Security of Encryption Keys

By Swati Joshi, Business Manager

The essence of secure communications is protecting the encryption key. While large encryption keys can provide a certain degree of protection against brute-force computational techniques to break a code, this protection does not address the need for physical security, which is equally important. To properly address physical security, several issues must be considered. These include: a physical mechanism for generating random keys, a physical design that prevents covert electronic interception of a key that is being communicated between authorized agents, and a secure method of storing a key that protects against clandestine physical and mechanical probing.

Using a host of features that range from package design, to external-sensor interfaces, to internal circuit architectures, Maxim's DS36xx family of secure supervisors provides all of these capabilities to military electronics design engineers. Devices with such features can simplify compliance with security requirements for both mature and emerging portable military computing and communications systems. The range of possible applications for these devices is, therefore, wide and diverse, as indicated in **Figure 1**.

Security Requirements for Electronic Data

The Federal Information Processing Standard (FIPS) is a standard that describes the U.S. government's requirements that cryptographic modules must meet for sensitive, but unclassified, uses. This standard is published by the National Institute of Standards and Technology (NIST). The FIPS 140-2 standard has four basic levels:

- Security Level 1: No Physical Security Mechanisms Required (Just Implements NIST Standardized Cryptographic Algorithms)
- Security Level 2: Tamper-Evident Physical Security
- Security Level 3: Tamper-Resistant Physical Security
- Security Level 4: Physical Security Provides an Envelope of Protection

For advanced-security military communication applications, designs must also meet National Security Agency (NSA) Type 1 certification standards. Equipment certified by the NSA is used to cryptographically secure classified U.S. government information. The certification process is rigorous and includes testing and analysis of the following items:

- Cryptographic Security
- Functional Security
- Tamper Resistance
- Emissions Security
- Security of Product Manufacturing and Distribution

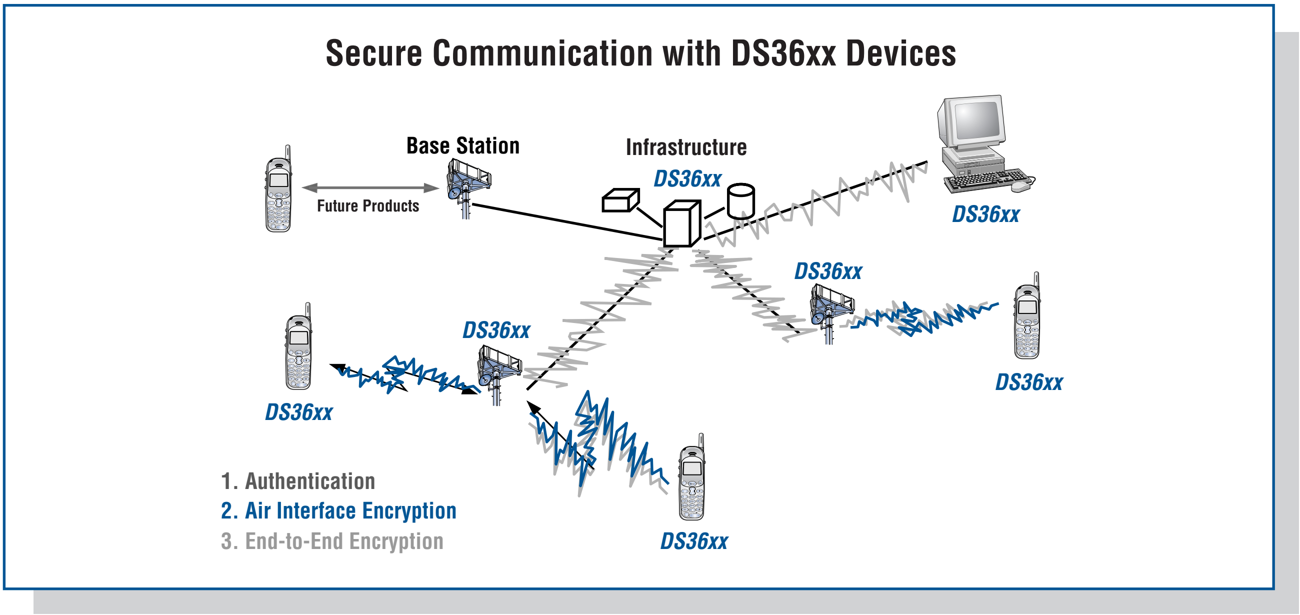


Figure 1. The DS36xx devices are suited for a wide range of present and future military and homeland security communications functions, including secure communications and client authentication.

A common example of an application that must comply with these guidelines is communications equipment designed to operate within the Warfighter Information Network-Tactical (WIN-T), which is the tactical communications protocol for warfighters. WIN-T supports a broad range of data, voice, and video capabilities. This network helps the warfighter stay connected at all times from any location by providing mobile, reliable, high-bandwidth communications. The capabilities provided by WIN-T are delivered by utilizing popular communications technologies, like a wireless local-area network (WLAN), voice-over-Internet protocol (VoIP), and third-generation cellular/satellite technology. WIN-T links warfighters located in tactical ground units with their commanders throughout the Department of Defense's (DoD's) worldwide network.

As with any military application, information security for WIN-T is extremely important. With WIN-T, the architecture must allow authorized users free access to the network, but also detect and deny unauthorized attacks. As such, WIN-T security must be built-in from the outset, rather than added on as an afterthought. This approach ensures safe and secure transmission of voice communications and digital data across the network.

In the past, systems were designed primarily for speedy deployment, often leaving security functions to be implemented as upgrades in the field. This happened because built-in security functions were usually considered to be quite expensive and a cause of schedule delays. However, all military communication applications now require a higher level of security from the outset to provide enhanced interoperability, connectivity, and regulatory compliance with FIPS 140-2, NSA, and WIN-T requirements. Security and intrusion prevention are increasingly crucial factors for other military applications as well. For example, General Dynamics®, together with Secure Computing®, recently developed the MESHnet Firewall for use in battlefield vehicles.

As a result, new military communications systems or components are no longer released without first meeting all of the applicable standards. Specifically, military communication applications are now required to meet, at a minimum, FIPS 140-2 Security Levels 3 and 4. Furthermore, in higher-level applications, the design engineer must adhere to NSA Type 1 and/or the newly implemented WIN-T requirements. Typically, at a minimum, military applications require a Security Level 3 certification for FIPS 140-2.

Achieving Compliance with Security Requirements

Addressing the security requirements set forth by the U.S. government is a complicated task for system designers. Security standards can (and should) change as often as the perceived threats for which they are developed, and generally become more stringent over time.

Keeping abreast of the ever-changing security standards can become troublesome for designers, because the design process must be guided by both the level of security required and the end purpose of the secure equipment to be designed. For example, security of an encryption key is not significantly increased by merely re-encrypting the keys, because sophisticated techniques have been developed to read encrypted keys. Therefore, keeping encryption keys secure from these techniques must be addressed using a combination of several different methods, including the enhancement of physical security.

When designing secure military systems that meet FIPS 140-2 (Security Levels 3 or 4), NSA Type 1, or WIN-T requirements, it is important to incorporate components that provide comprehensive tamper protection, even in the absence of main power. Members of Maxim's DS36xx family, such as the DS3600 shown in **Figure 2**, offer integrated solutions to secure both encryption keys and critical data by actively detecting tampers, even while on battery power (which engages immediately and transparently in the absence of main power). The on-chip power-supply monitor and battery switch ensure that all tamper-detection mechanisms remain active, regardless of the power source. Main power is constantly monitored—when it falls below the low threshold, an external backup battery is instantly and automatically switched in to keep both the internal and external protection circuitry alive. Thus, tamper detection is not interrupted with the loss of the equipment's main power source.

To comply with the requirements of FIPS 140-2 (Security Levels 3 and 4), as well as the NSA Type 1 and WIN-T specifications, tamper detection components must allow the designer to attach their own external sensors, so that an envelope of protection—that is, a security boundary—can be provided around the devices storing the protected data. Attaching external sensors to the DS36xx series, the system designer has a unique and flexible method for adding layers of security to the application, thereby meeting many of the applicable requirements set forth by governing agencies.

To meet these various governmental requirements, analog supply voltages, digital signals, and a resistive-mesh protective sensor grid can all be easily and simultaneously

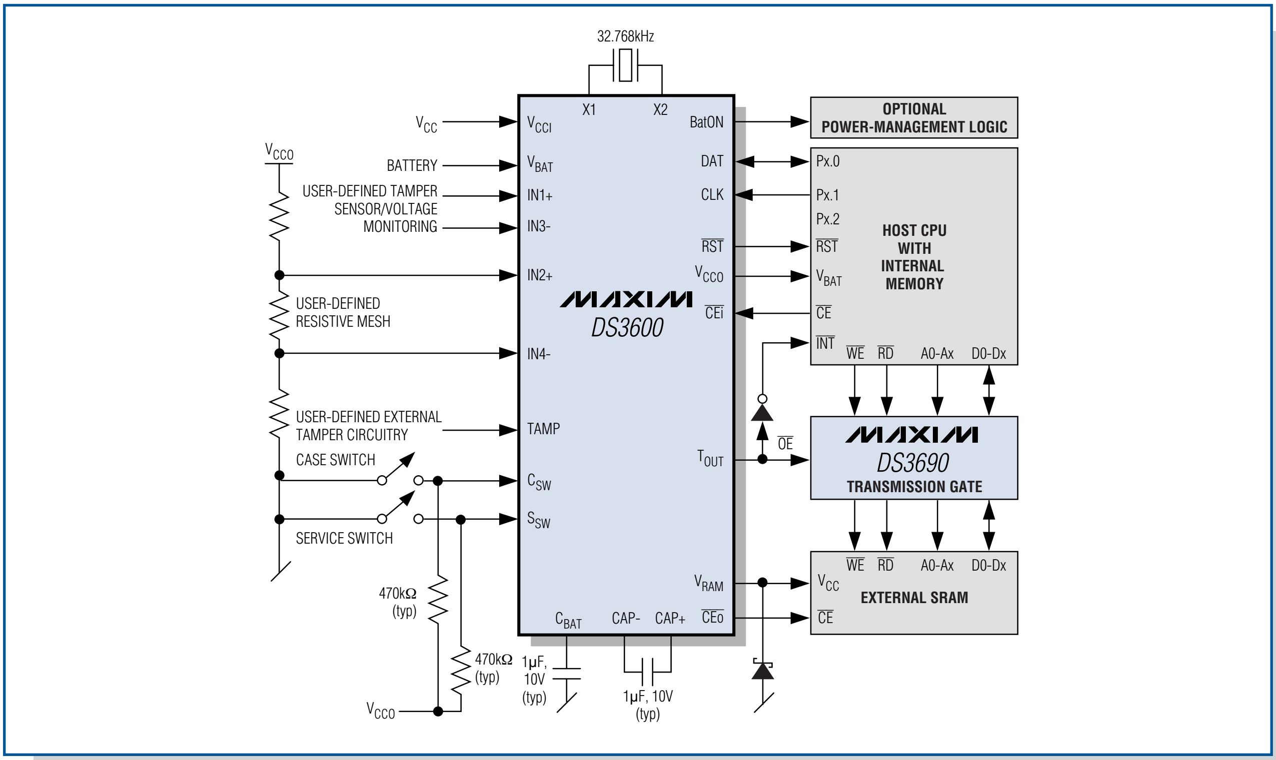


Figure 2. The DS3600 secure supervisor uses a combination of features and mechanisms to detect tampering and protect the contents of battery-backed volatile memory, such as internally stored encryption keys, or other sensitive data stored in an external SRAM.

monitored by the DS36xx secure supervisors. Furthermore, all DS36xx devices are offered in chip-scale ball-grid-array (CSBGA) packages (see **Figure 3**). By severely restricting access to the pins of a mounted device, these packages provide yet another layer of passive physical security for the control and data signals.

Internal Security Features

The DS36xx devices also include additional layers of protection in the form of internal tamper-detection mechanisms. These internal mechanisms compliment the device's ability to interface to a customized configuration of external tamper-detection sensors. The internal tamper-detection mechanisms, which include an on-chip temperature sensor, case-switch monitor, power-supply monitor, battery monitor, and oscillator monitor, provide continuous tamper-detection monitoring. This monitoring remains active at all times, especially when running on battery power.

As with the external mechanisms, the internal mechanisms are triggered when user-defined and/or factory-programmed thresholds are violated. For example, in order to meet the prerequisites of certification bodies, such as the NSA, and those governing the FIPS and WIN-T standards, the designer can use the internal temperature sensor, which monitors the substrate temperature. Once either the upper or lower temperature limits are violated, a tamper response is initiated by the device.

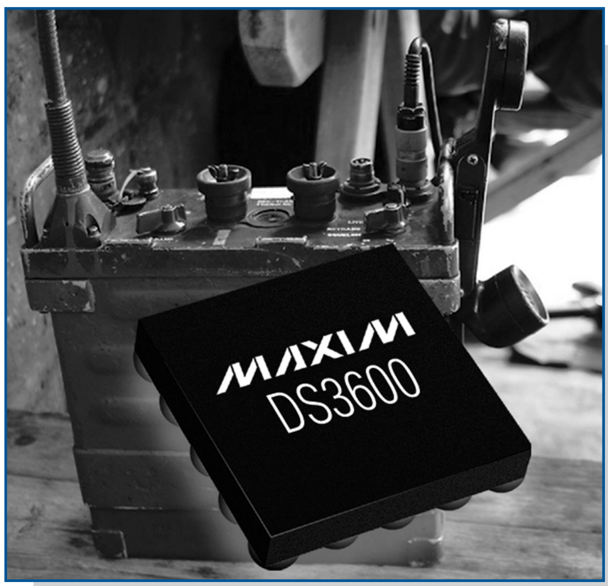


Figure 3. The CSBGA package of the DS36xx family provides a layer of passive protection by limiting access to I/O signals when the device is installed on a circuit board.

Besides measuring instantaneous temperature, an additional temperature-monitoring function is provided by the DS36xx devices. Specifically, a rate-of-change detector monitors the speed at which the substrate temperature changes. A rapid increase or decrease in temperature triggers a tamper response in the device, which provides additional protection against advanced, clandestine data-recovery techniques.

One documented method of recovering data from protected SRAM involves the application of liquid nitrogen prior to the removal of power to the device. This procedure extends the data retention of nonpowered SRAM cells to the millisecond timescale. However, the temperature monitoring provided by the DS36xx family would interpret this action as a tampering event, and the device would erase its internal memory before the onset of this cryogenic memory-retention effect. The memory is hardwired to provide a high-speed-clear function that completely resets the entire memory array in less than 100ns. This function can also be triggered by other tamper events (such as an interlock breech) or through a direct command sent to the device's I^2C-/SPI™ -compatible interface.

The DS36xx devices also include a proprietary feature called nonimprinting key memory.† Specifically, nonimprinting key memory addresses the security risk created by the tendency of SRAM memory cells to exhibit charge accumulation or depletion (depending on the data that is stored) in the oxide layers of the devices composing the memory cells. Data stored in these conventional memory cells over a long period of time causes oxide layers to become stressed, and subsequently leaves an imprint of the data that was stored there. This data can be read even after the cells have been cleared.

However, nonimprinting key memory technology has been designed and developed to eliminate the phenomenon of oxide stress. The technology works by continuously complementing the device's conventional battery-backed SRAM memory. Therefore, when the memory is cleared as a result of a detected tamper event or through a direct command, the entire memory is cleared and no trace of the data that resided there will be present. This function offers the designers of military and government products a unique and extremely secure method for storing highly sensitive encryption keys.

Response to Tamper Events

The DS36xx devices constantly monitor all of the previously described tamper inputs and events. When tampering is detected, either through the internal or external tamper-detection mechanisms, a tamper response is immediately generated. The tamper event starts with identification of the tamper source. The tamper latches remain frozen until the condition causing the tamper event has been cleared. Then the tamper latches a reset. **Table 1** outlines the specific sequence of actions taken by the DS36xx devices during a tamper response.

Supporting Secure Military Applications

In addition to the physical security needed to protect a stored encryption key, physical security is also needed in the actual generation of an encryption key. That is, the method used to generate a digital encryption key must ensure that an unauthorized copy of the key cannot be regenerated, either by the same equipment (which would defeat the purpose of secure data storage provided by the DS36xx family), or by an exact replica of the equipment.

The random-number-generator (RNG) function of the DS36xx devices is a deterministic pseudorandom algorithm, which is seeded using two sources of natural randomness generated on chip. This function provides a continuous bitstream that is intended to be post-processed by the host CPU to form the seed for a certified software RNG function. Furthermore, each DS36xx secure supervisor contains a factory-programmed unique silicon serial number, which is readable through the I/O port. The silicon-inscribed serial number offers the user a method to uniquely identify each end product.

Additionally, the newer DS36xx devices can erase certain specific memory cells based on the type of tamper that occurred. This function is referred to as erasure hierarchy (see **Table 2** for devices), and is useful for applications in which the integrity of the equipment is still intact. That is, one can still use the equipment to a certain degree after the tamper has occurred, though all of the functions may not be available. One such application is a communications device, such as a secure military radio, that must remain somewhat operational although a tamper event has occurred.

Table 1. Sequence of Actions Taken when a DS36xx Device Detects a Tamper Event

Step	Action
1	The internal encryption key is immediately, completely, and actively erased (if applicable).
2	The external RAM is erased (if applicable).
3	The tamper-latch registers record the state of the tamper input sources.
4	The tamper output asserts to alert the system processor.
5	The tamper-event time-stamp register records the time of the tamper event.

Besides providing high levels of data security, many defense applications are also required to withstand a wide temperature range during both operation and storage. While the DS36xx devices are intended to provide high security in conventional ambient operating environments, some of the newer products in this family also support wider operating temperature ranges that approach the extremes defined by the full military temperature range (-55°C to +95°C for the DS36xx versus -55°C to +125°C for the full military range).

Conclusion

As shown in Table 2, the DS36xx family of secure supervisors provides a wide range of capabilities, enabling systems that can generate and store encryption keys, monitor for tamper events, and actively and completely destroy the keys when a tamper event is detected. Additionally, by making use of the external inputs provided by the DS36xx devices, the system designer can add more layers of security to an application to meet the requirements set forth in mandates relating to the FIPS, NSA, and WIN-T.

Table 2. DS36xx Devices and Their Distinctive Features

Part	I/O	No. of Analog Voltages Monitored	No. of Digital Inputs Monitored	Operating Temperature Range (°C)	Internal Key Memory (Bytes)	External Memory Control	Random Number Generator	Overvoltage Monitor	Battery Monitor	Erasure Hierarchy
DS3600	3-wire	4	1	-40 to +85	64	✓	✓		✓	
DS3605	I^2C	4	1	-40 to +85	N/A	✓	✓		✓	
DS3640	I^2C	5	3	-40 to +85	1k		✓	✓	✓	
DS3641	4-wire	5	3	-40 to +85	1k		✓	✓	✓	
DS3644*	I^2C	12	4	-55 to +95	1k	✓	✓	✓	✓	2 levels
DS3645*	I^2C	12	4	-55 to +95	4k	✓	✓	✓	✓	
DS3650	4-wire	2	N/A	-40 to +85	N/A			✓	✓	
DS3655*	I^2C	N/A	4	-40 to +85	64					
DS3665*	SPI	12	4	-55 to +95	8k	✓	✓	✓	✓	4 levels

†Patent pending.
*Future product—contact factory for availability.

Cookbook for Analog Video Filtering in Camera Systems

By Ben Nader, Strategic Applications Engineer

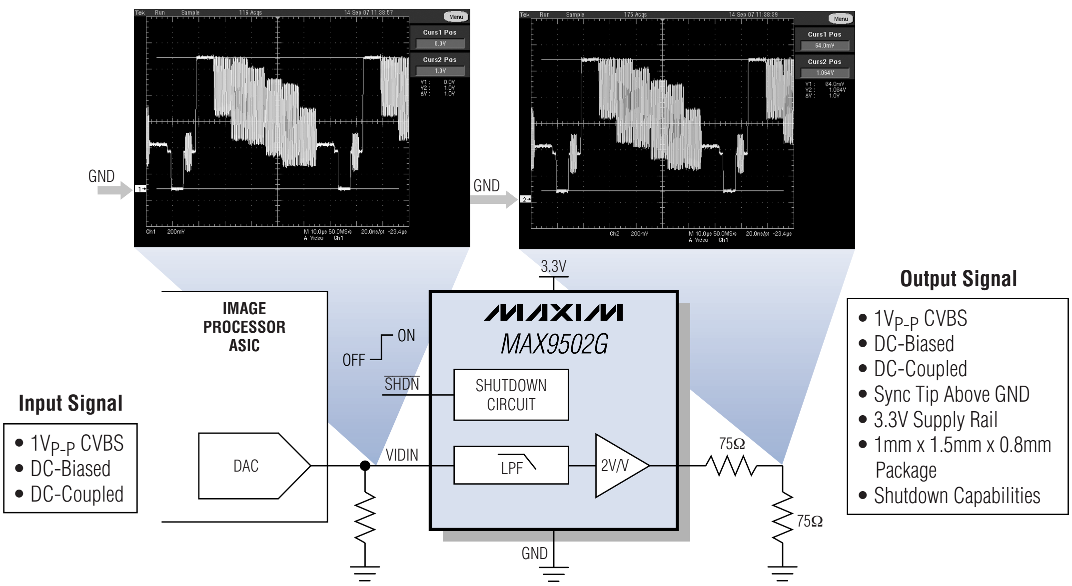
In most video systems, lowpass filters are included on the video output lines of the video encoders. These filters reject high-frequency noise and smooth out the rising-/falling-edge video signals that are output from a video digital-to-analog converter (DAC). Traditionally, discrete passive filters have been used in such configurations. However, in most of today's video subsystems, an integrated filter amplifier follows the video DAC to clean up and amplify the video signal. This article details Maxim's variety of integrated video filter amplifiers that satisfy a wide range of video application requirements.

In video-camera applications, the most common signals that video DACs output are composite video blanking and sync (CVBS) and luminance/chrominance (Y/C) signals. The eight filter amplifier configurations detailed in **Examples 1** through **8** are composed of different combinations of the signal's DC level at the DAC output, signal amplitude, and AC- or DC-coupling of the video signal. Common power-supply rails for integrated video filters are 5V or 3.3V. However, for the applications with the lowest power requirements (Examples 6 and 7), a video filter amplifier can be powered by a 1.8V or 2.5V supply. The specific filter amplifier (MAX9509) used in these low-power examples takes advantage of Maxim's patented DirectDrive™ technology,† and delivers a $2V_{P-P}$ video signal with an internal fixed gain of 8V/V.

The following eight configurations have several common features. All outputs are measured at 75Ω loads. Thus, when the output graph shows $1V_{P-P}$, the output of the integrated filter amplifier should be $2V_{P-P}$. Also, a 75% TV NTSC color-bar signal is used as the source for all filter examples.

Example 1

Reconstruction Filter Connects the Video DAC to the Video Amplifier

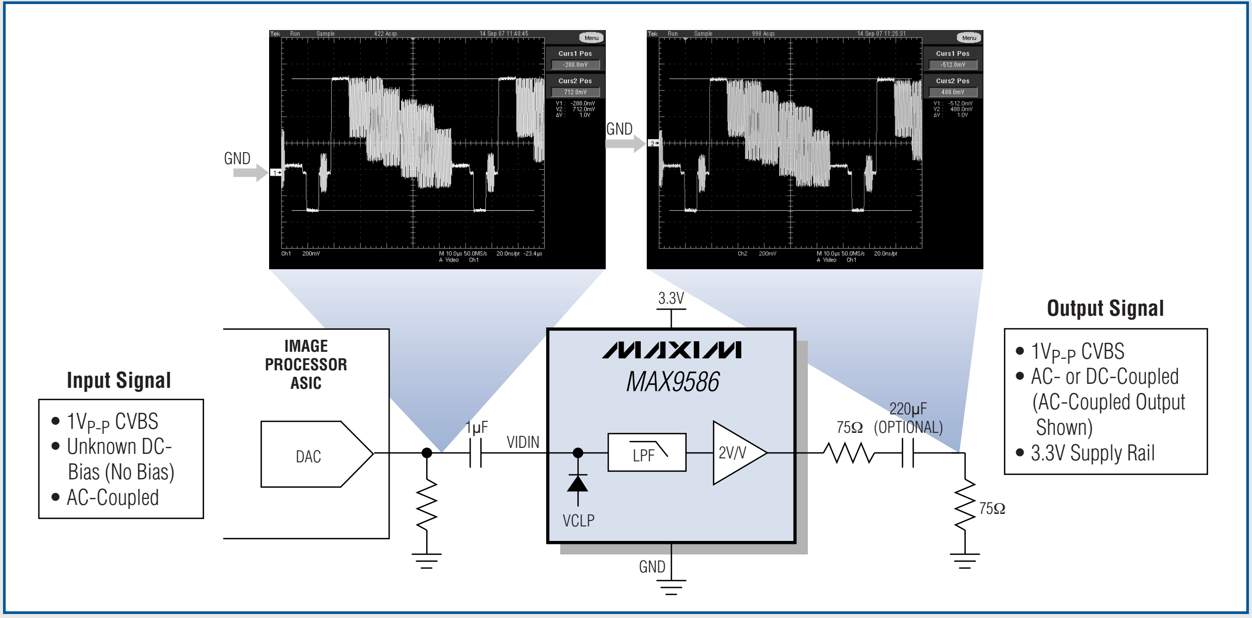


Note: This solution is not recommended if AC-coupling capacitors are required on the video output line; in that situation, designers should seek a different solution.

In Example 1, the video DAC's output connects to a MAX9502G video amplifier with a reconstruction filter. The DAC's video signal output is biased so that the sync tip is near ground. The MAX9502G filters and boosts the signal, and then delivers a $2V_{P-P}$, DC-biased signal. The output of MAX9502G is also biased and its sync tip is approximately 300mV above ground. This sync-tip value changes to 150mV at the load due to the 75Ω divider setup at the output. A highly-integrated solution, the MAX9502G consumes little board area, thus saving space in most portable system designs.

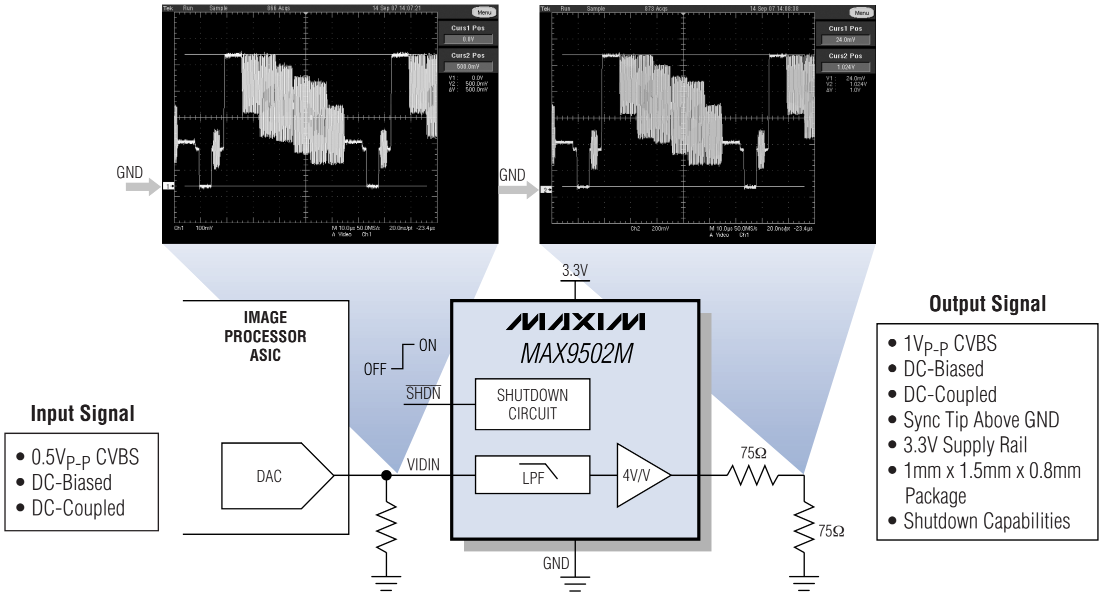
Video DAC Sends an AC-Coupled Signal to the Video Amplifier

Example 2



In Example 2, a video DAC delivers an AC-coupled video signal to the MAX9586 video filter amplifier. This is a good solution for single-supply applications that require the signal to be AC-coupled and the sync tip to be placed below ground. However, AC-coupling the video at the output does not put the black level at ground; instead, the black level changes as the content of the video signal changes. The MAX9586 can drive two DC-coupled video loads or a single AC-coupled 150Ω load.

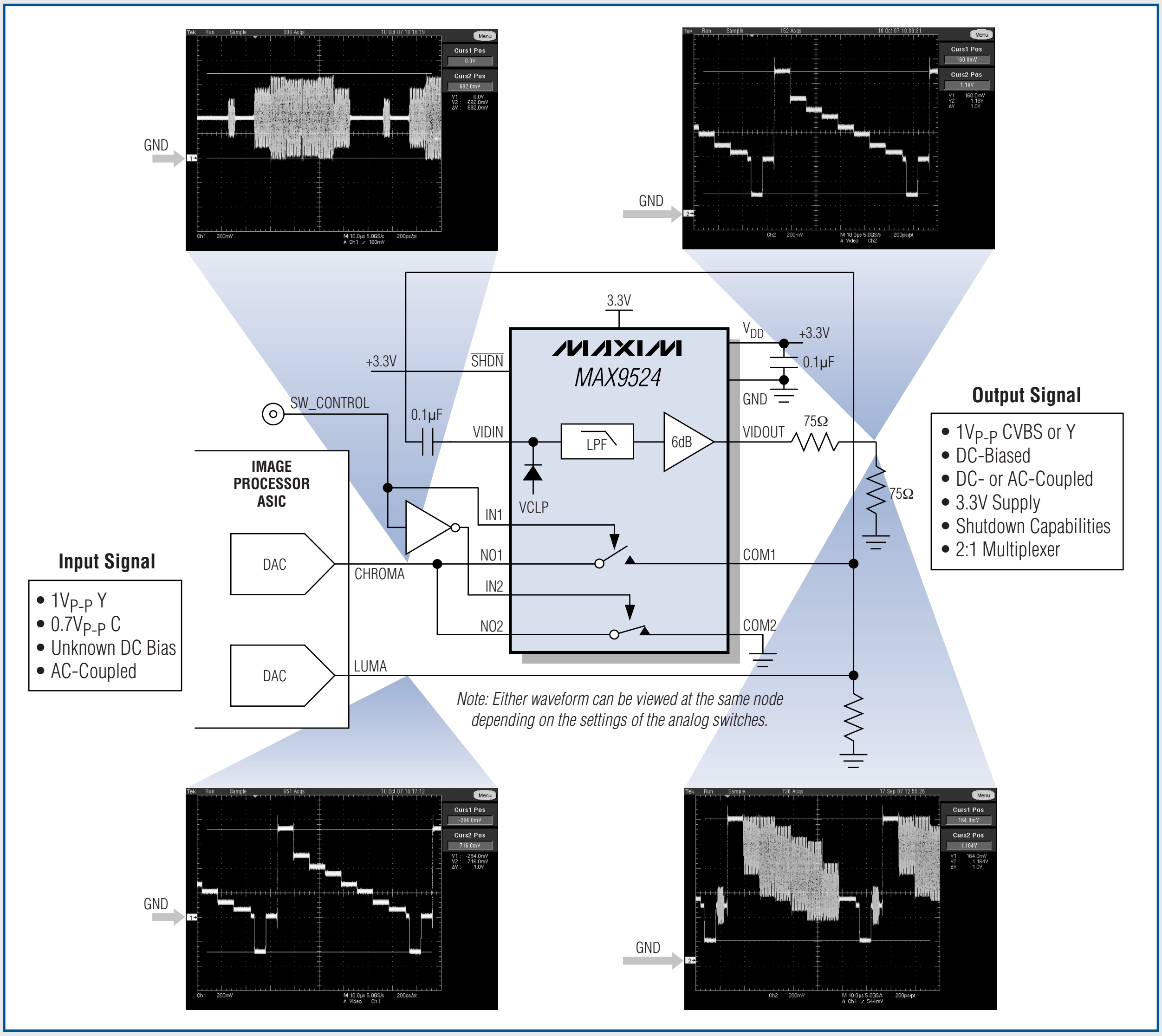
Example 1 with a 0.5V$_{P-P}$, DC-Biased Signal



Note: This solution is not recommended if the design requires AC-coupling capacitors on the video output line; if this is the case, designers should seek a different solution.

Example 3 is very similar to Example 1, except that the DAC can only output a 0.5V$_{P-P}$, DC-biased signal. The MAX9502M is the appropriate solution in this case because of its 12dB fixed gain. The video signal at the load has a DC offset and the sync tip is about 150mV above ground. Also, the video signal output from the DAC must be above ground. The MAX9502M can drive a 2V$_{P-P}$ video signal into a 150Ω load to ground.

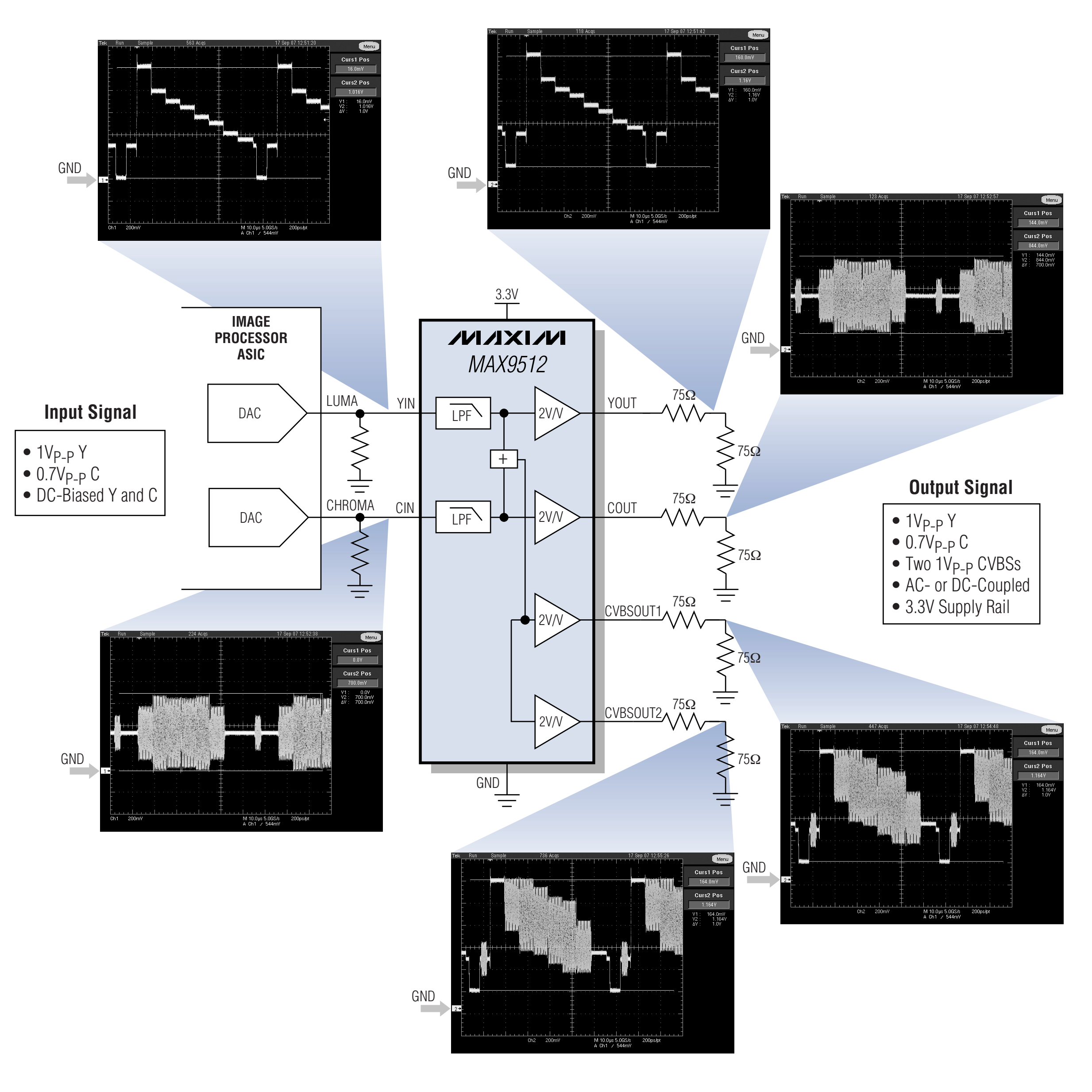
Video DAC with Only One Output Line for CVBS or Y Signals



Example 4 is an interesting configuration. In certain applications, DACs provide both Y and C, but the Example 4 design has only one output line. This output should be selectable between CVBS and Y signals so that a CVBS signal can be created by using a summer (combiner) circuit. It is difficult to provide both types of signals on the same output line and switch between them at the appropriate time. This is usually done by implementing a 2:1 multiplexer on the output line. Fortunately, the MAX9524 video filter amplifier used in this example has two integrated analog single-pole switches that can be set up as a 2:1 multiplexer. This is very useful, as this single integrated chip can both select the appropriate input and filter-amplify it. The DC level is unknown because of the summation of Y and C; therefore, the video signal should be AC-coupled before the filter-amplifier. The clamp circuitry after the AC-coupling capacitor sets the bias level.

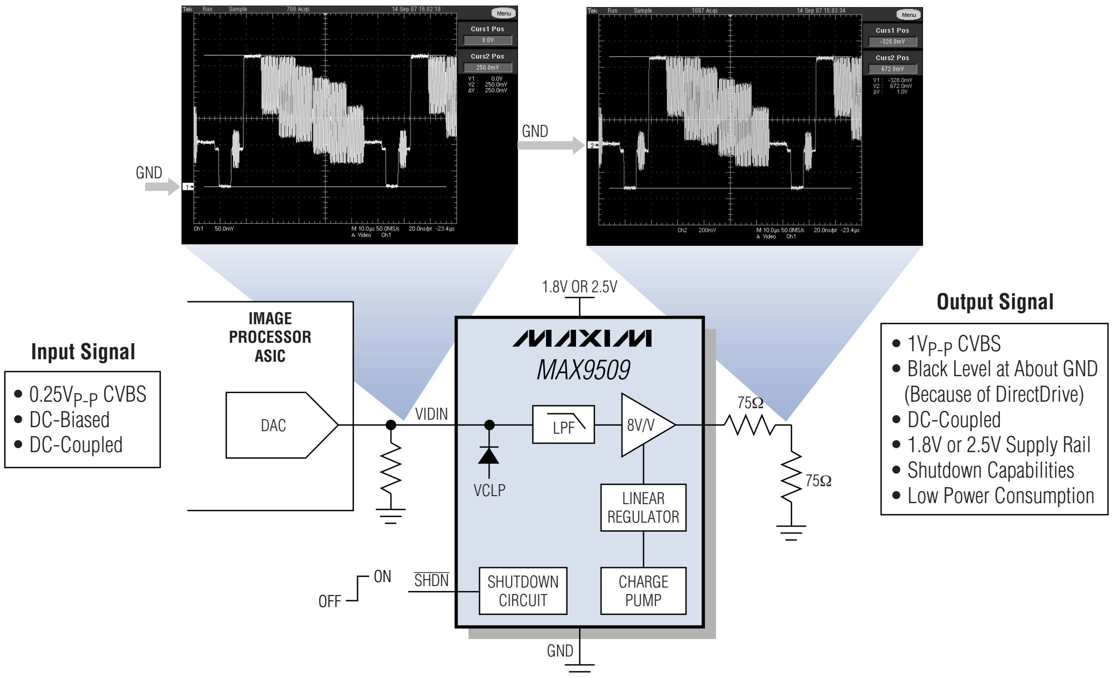
Designers should pay close attention to the combiner circuit that creates the CVBS signal. The DC offset levels of Y and C, as well as the DAC's voltage-compliance level, should be taken into careful consideration. Directly connecting Y and C, depending on the DC-bias level of each signal, could create a CVBS signal that extends beyond the DAC's voltage-compliance range.

Multiple Video Outputs with a Y/C-to-CVBS Mixer



Example 5 is appropriate for designs with multiple video outputs, as the MAX9512 has four separate output channels. This device also has a Y/C-to-CVBS mixer, which creates a composite video signal from Y and C. Each output is capable of driving two DC-coupled video loads or an AC-coupled 150Ω load. This chip also has Maxim's SmartSleep circuitry‡ (not shown) that can detect input signals or output loads and reduce power consumption by turning on/off different amplifiers accordingly. This configuration can most commonly be used to provide an S-video output, as well as two CVBS outputs.

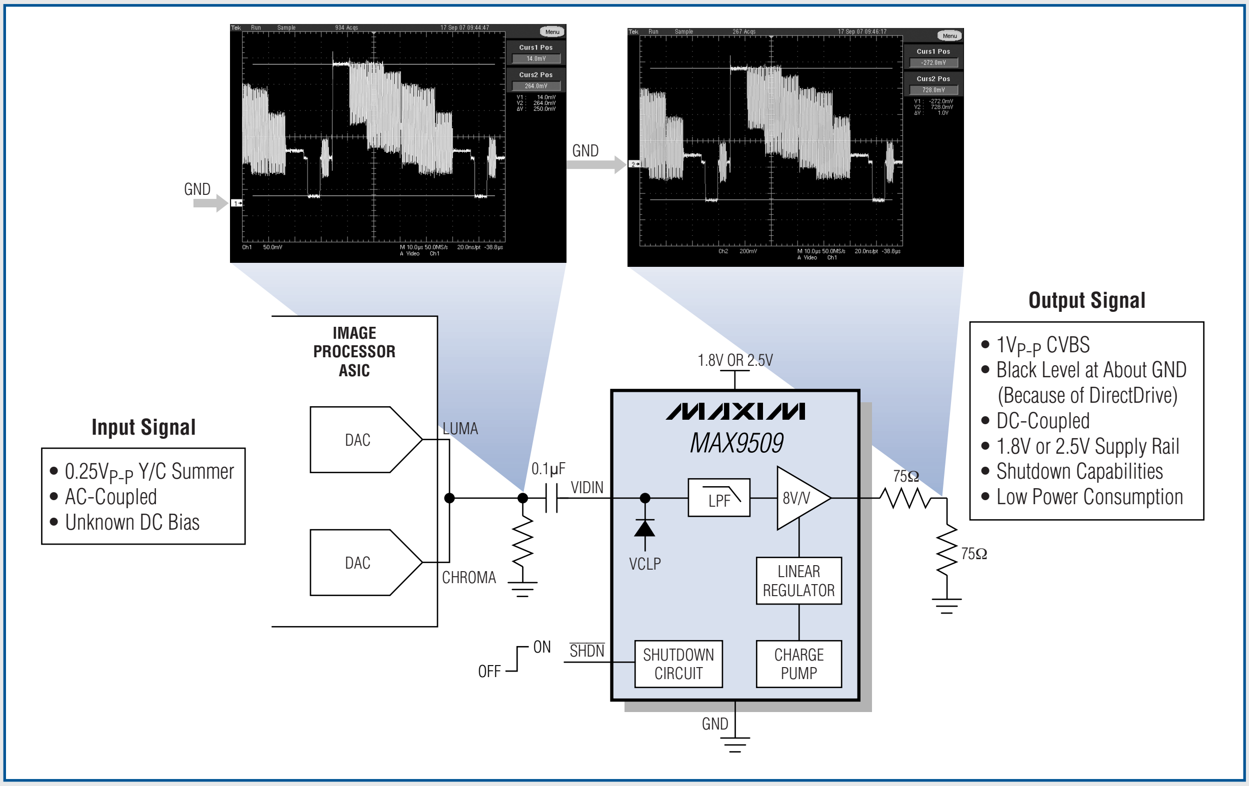
Low Power Consumption with a Black Level Nearly at Ground



Note: Video DACs with a $1V_{P-P}$ output signal can work in this configuration if the DAC's output terminating resistor is scaled down.

Example 6 minimizes power consumption by leveraging the MAX9509, which operates from a single 1.8V supply and consumes 11.7mW average power. Other advantages of this configuration are that the black level is almost at ground without the need for a large coupling capacitor on the output, and that the video signal is between -300mV and +700mV independent of the video signal contents. Because the amplifier has an internal fixed gain of 8V/V, the DAC output should have an amplitude of $0.25V_{P-P}$. This can easily be achieved by changing the value of the terminating resistor at the output of any type of DAC.

Y, C, and CVBS Signals from One Output

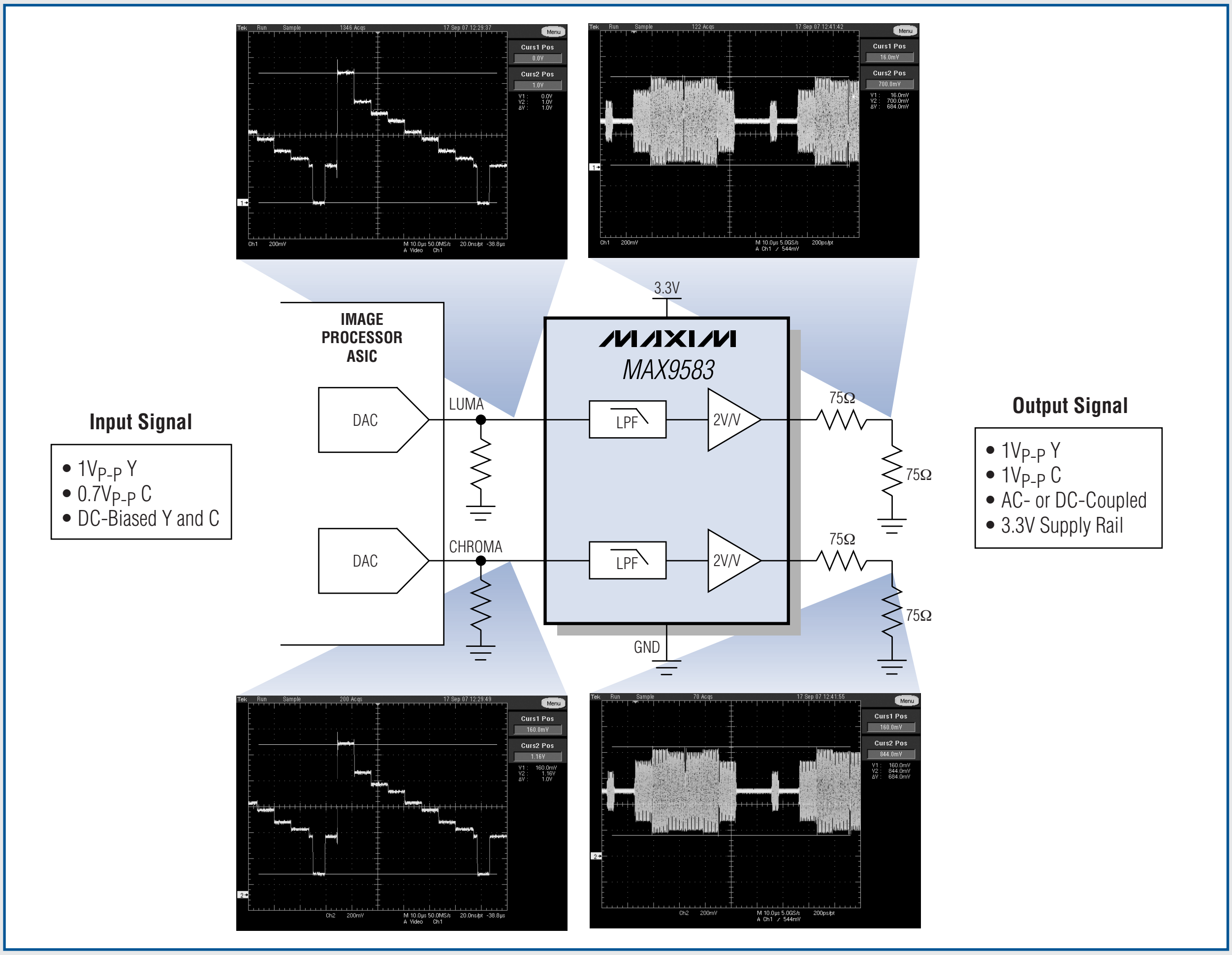


For certain applications, only Y and C signals are available on the DAC's output, but the system must still deliver a CVBS signal. In such situations, a common solution is to use a combiner circuit to create the desired output signal. This common solution is similar to the combiner circuit in Example 4, but because the amplitude of the desired CVBS is only $0.25V_{P-P}$, meeting voltage compliance levels is probable. If the DAC normally outputs $1V_{P-P}$, an amplitude of $0.25V_{P-P}$ can easily be achieved by changing the value of terminating resistor at the DAC.

Example 7 demonstrates the appropriate filtering-amplifying solution for a very low-power application. The designer can obtain the appropriate amplitude ($0.25V_{P-P}$) by scaling down the terminating resistor at the DAC output. Because the DC bias level can be unknown (depending on the signals and combiner circuit), the signal should be AC-coupled into the MAX9509. A sync-tip clamp level-shifts the signal appropriately at the input. Because of the filter-amplifier's DirectDrive capabilities, the black level at the amplifier's output is sitting approximately at ground. This eliminates the need for large coupling capacitors on the output. The MAX9509 can, therefore, drive a $2V_{P-P}$ video signal into a 150Ω load.

Two Video Output Signals with No DC Offset

Example 8



For applications that require two video output signals (such as S-video), the MAX9583 two-channel video filter amplifier provides the compact solution seen in Example 8. The MAX9583 has an internal fixed gain of 2V/V and, therefore, is suited for DACs with a $1V_{P-P}$ output. The output of this device can be AC-coupled to a 150Ω load or two DC-coupled video loads. AC-coupling of the video signal eliminates any DC offset, and the black level changes as the video content changes.

Conclusion

This article focuses on most of the common configurations seen in today's video-camera applications. CVBS and Y/C are by far the most common output signals in such applications. Rarely, on some of the higher end equipment, one might see a YPbPr output whether the video signal is standard definition (SD) or high definition (HD). Though this article does not discuss these rare applications, designers should be aware that there are integrated solutions available.

†U.S. Patent #7,061,327.
‡Patent pending.

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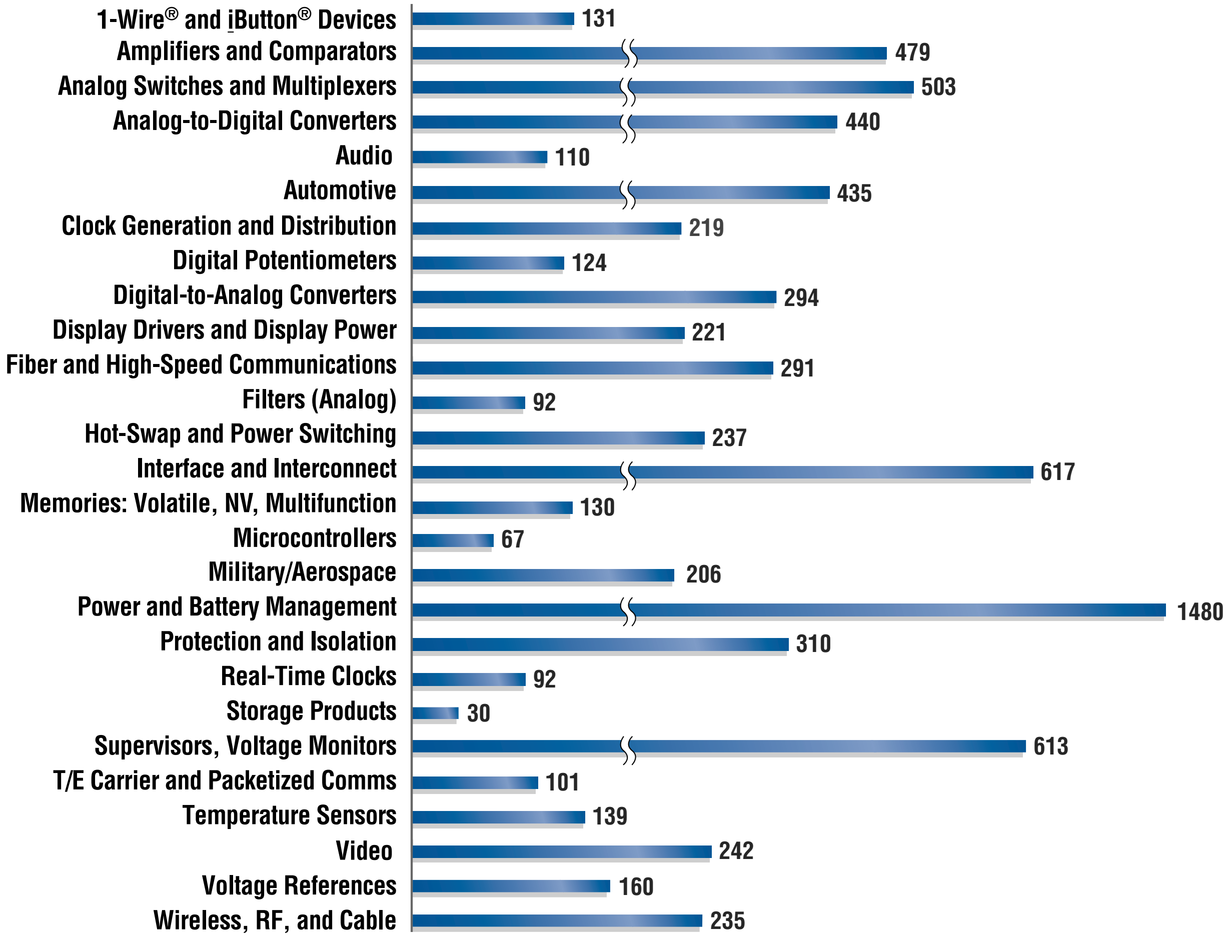

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